

HM6709A Series

65536-word × 4-bit High Speed Static Random Access Memory

Features

- 65536-words × 4 bit organization
- Fully TTL compatible input and output
- 1.0 μm Hi-BiCMOS process
- +5 V single supply
- Completely static memory
No clock or timing strobe required
- Low power dissipation
Operating: 400 mW typ
- Super fast
Address access time: 15/20 ns (max)
 \overline{OE} access time: 7/10 ns (max)

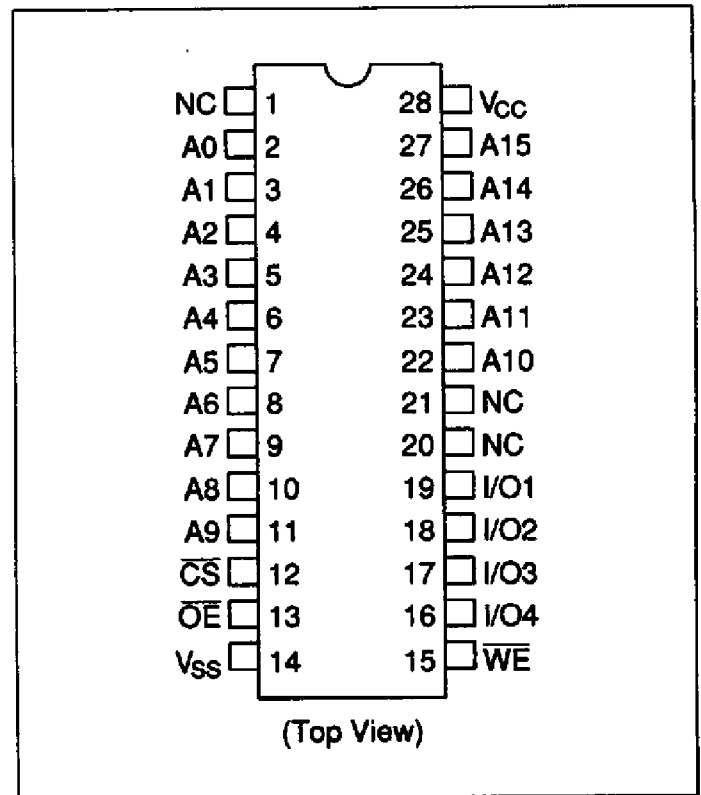
Ordering Information

Type No.	Access time	Package
HM6709AJP-15	15 ns	300-mil 28-pin plastic SOJ
HM6709AJP-20	20 ns	(CP-28DN)

Pin Description

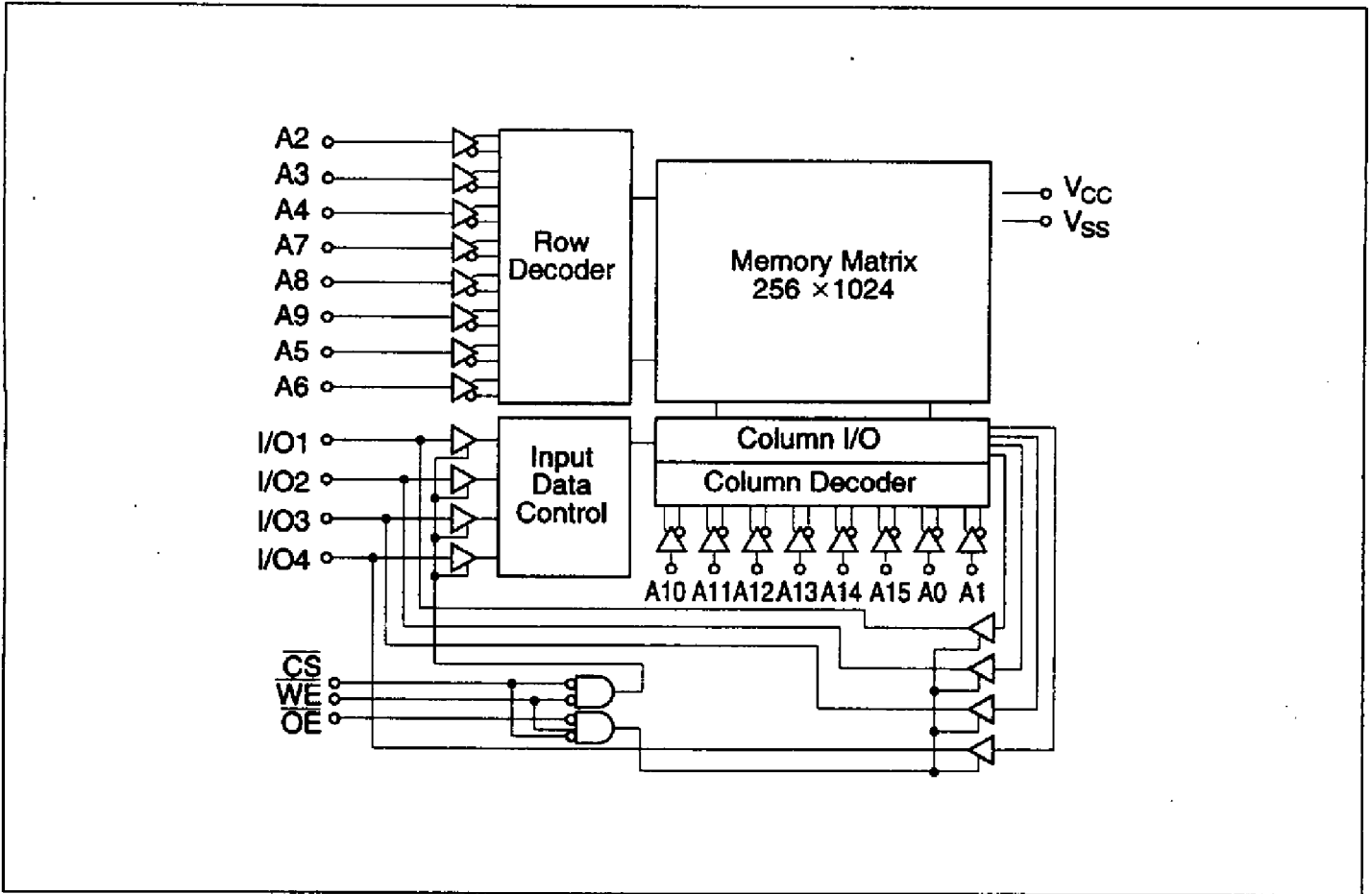
Pin name	Function
A0 – A15	Address input
I/O1 – I/O4	Data input/output
WE	Write enable
\overline{CS}	Chip select
\overline{OE}	Output enable
V _{SS}	Ground
V _{CC}	Power supply

Pin Arrangement



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Block Diagram



Function Table

\overline{CS}	\overline{WE}	\overline{OE}	Mode	I/O pin	V_{CC} current	Ref. cycle
H	X	X	Not selected	High-Z	I_{SB}, I_{SB1}	—
L	H	H	Output disable	High-Z	I_{CC}, I_{CC1}	—
L	H	L	Read	Data out	I_{CC}, I_{CC1}	Read cycle (1), (2), (3)
L	L	H	Write	Data in	I_{CC}, I_{CC1}	Write cycle (1), (2), (3), (4)
L	L	L	Write	Data in	I_{CC}, I_{CC1}	Write cycle (5), (6)

Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Terminal voltage to V _{SS} pin	V _T	-0.5 to +7.0	V
Power dissipation	P _T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	-10 to +85	°C
Storage temperature range	Tstg	-55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0.0	0.0	0.0	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input low voltage	V _{IL}	-3.0 ^{*1}	—	0.8	V

Note: 1. Pulse width 15 ns, DC : -0.5 V

DC Characteristics ($V_{CC} = 5.0V \pm 10\%$, $T_a = 0$ to $+70^\circ C$)

Parameter	Symbol	HM6709A-15			HM6709A-20			Unit	Test conditions
		Min	Typ	Max	Min	Typ	Max		
Input leakage current	$ I_{LI} $	—	—	2	—	—	2	μA	$V_{CC} = 5.5 V$, $V_{in} = 0 V$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	10	—	—	10	μA	$\overline{CS} = V_{IH}$ or $OE = V_{IH}$, $WE = V_{IL}$ $V_{I/O} = 0 V$ to V_{CC}
Operating power supply current	I_{CC}	—	—	100	—	—	100	mA	$\overline{CS} = V_{IL}$, $I_{I/O} = 0 mA$
Average operating current	I_{CC1}	—	—	140	—	—	120	mA	min. cycle, Duty : 100%, $I_{I/O} = 0 mA$
Standby power supply current	I_{SB}	—	—	30	—	—	30	mA	$\overline{CS} = V_{IH}$, $V_{in} = V_{IH}$ or V_{IL}
	I_{SB1}	—	—	10	—	—	10	mA	$\overline{CS} \geq V_{CC} - 0.2 V$ $V_{in} \leq 0.2 V$ or $V_{in} \geq V_{CC} - 0.2 V$
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	$I_{OL} = 8 mA$
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	$I_{OH} = -4 mA$

Capacitance ($T_a = 25^\circ C$, $f = 1 MHz$)

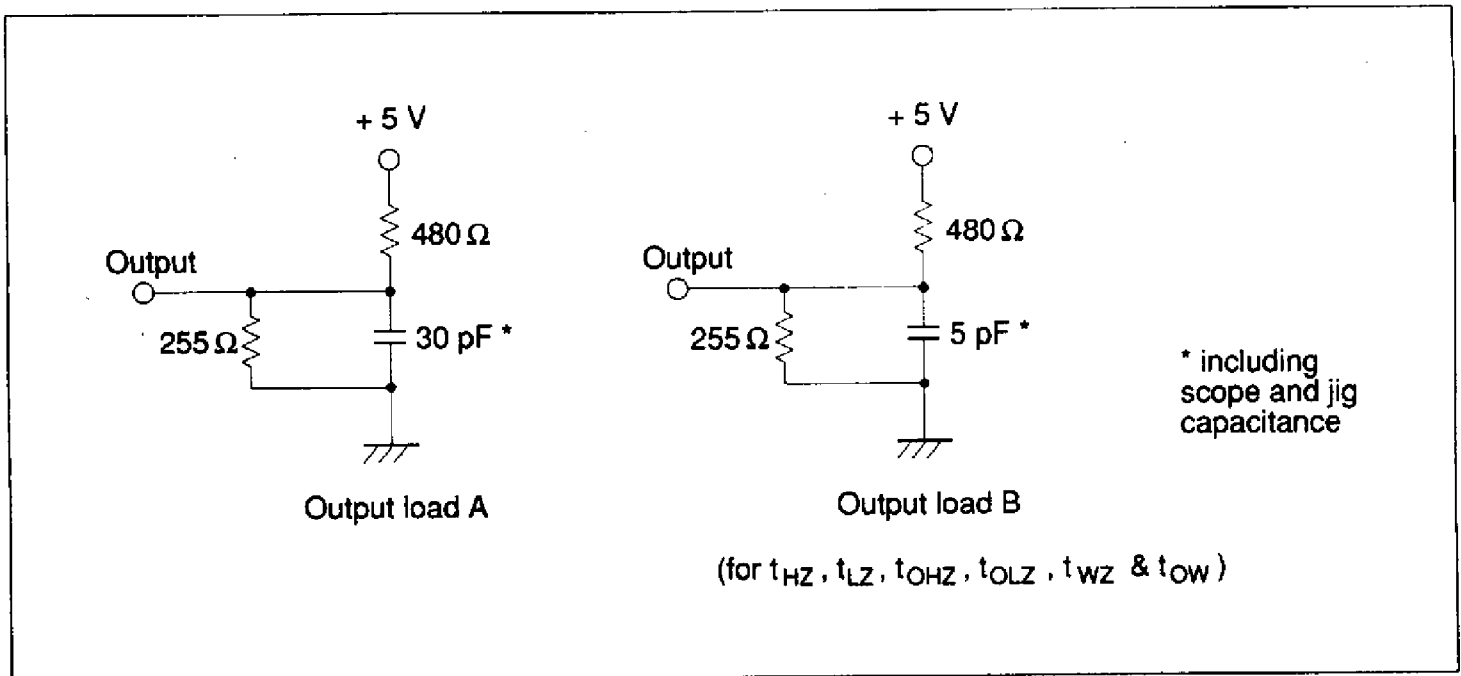
Parameter	Symbol	Max	Unit	Test condition
Input capacitance	C_{in}^{*1}	6	pF	$V_{in} = 0 V$
Input/output capacitance	$C_{I/O}^{*1}$	10	pF	$V_{I/O} = 0 V$

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figures
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



Read Cycle

Parameter	Symbol	HM6709A-15		HM6709A-20		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip select access time	t_{ACS}	—	15	—	20	ns
Chip selection to output in low-Z	$t_{LZ}^{*1, *2}$	4	—	4	—	ns
Output enable to output valid	t_{OE}	0	7	0	10	ns
Output enable to output in low-Z	$t_{OLZ}^{*1, *2}$	0	—	0	—	ns
Chip deselection to output in high-Z	$t_{HZ}^{*1, *2}$	0	6	0	8	ns
Output hold from address change	t_{OH}	4	—	5	—	ns

- Notes: 1. This parameter is sampled and not 100% tested.
 2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

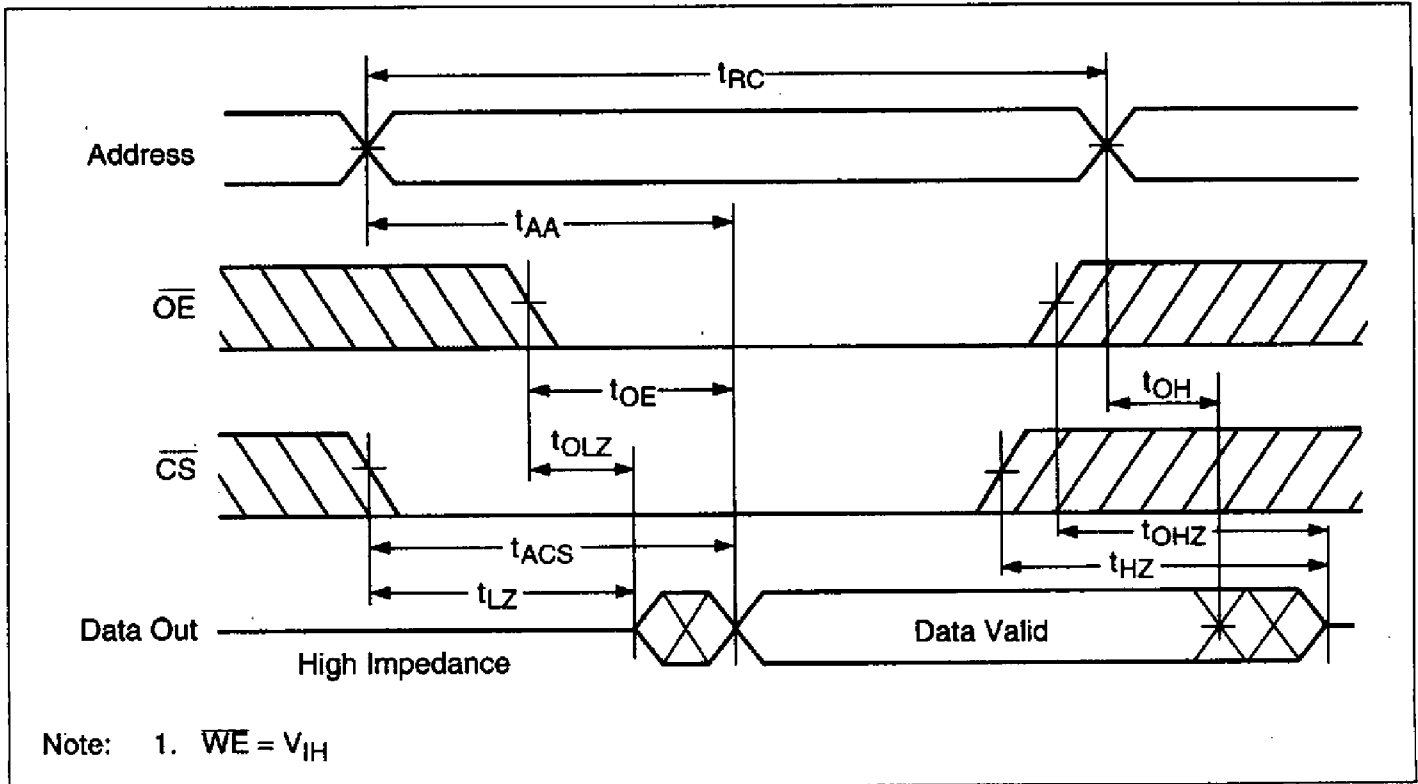
Write Cycle

Parameter	Symbol	HM6709A-15		HM6709A-20		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}^{*1}	15	—	20	—	ns
Chip selection to end of write	t_{CW}	10	—	15	—	ns
Address valid to end of write	t_{AW}	10	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	15	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	8	—	10	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enable to output in high-Z	$t_{WZ}^{*2, *3}$	0	6	0	8	ns
Output disable to output in high-Z	$t_{OHZ}^{*2, *3}$	0	6	0	8	ns
Output active from end of write	$t_{OW}^{*2, *3}$	0	—	0	—	ns

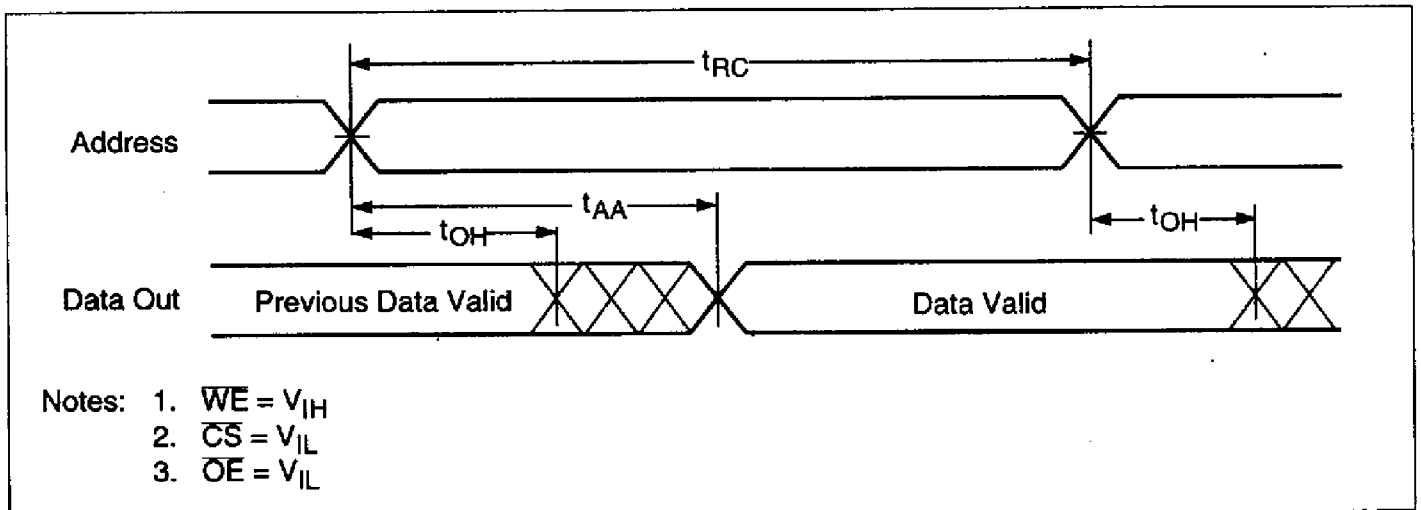
- Notes:
1. All write cycle timings are referenced from the last valid address to the first transitioning address.
 2. This parameter is sampled and not 100% tested.
 3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

Timing Waveforms

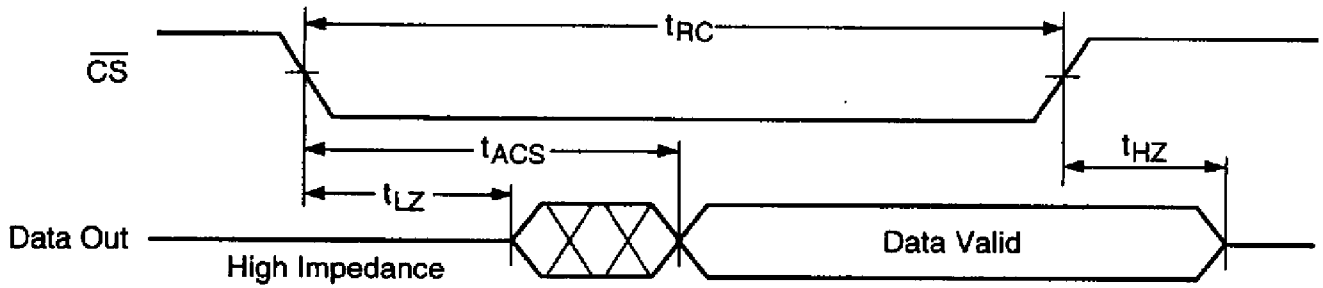
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

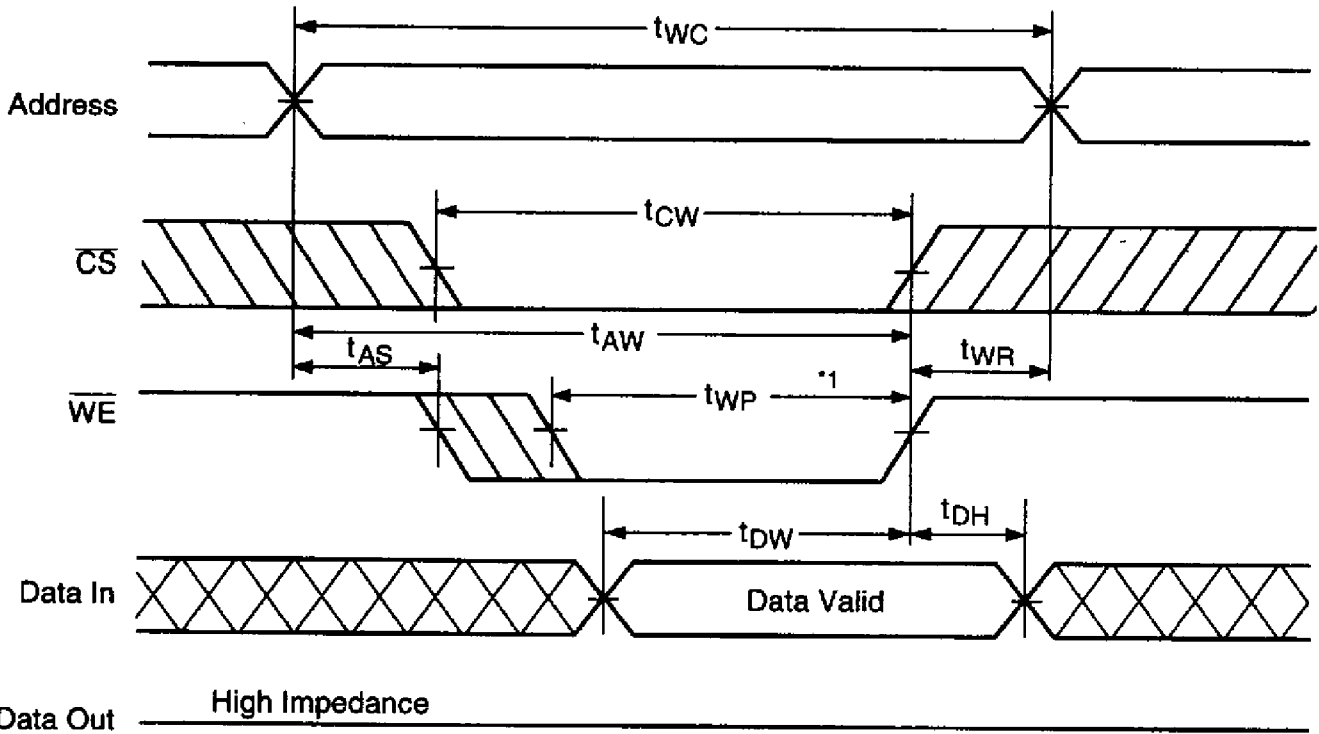


Read Cycle (3) *1, *2, *3



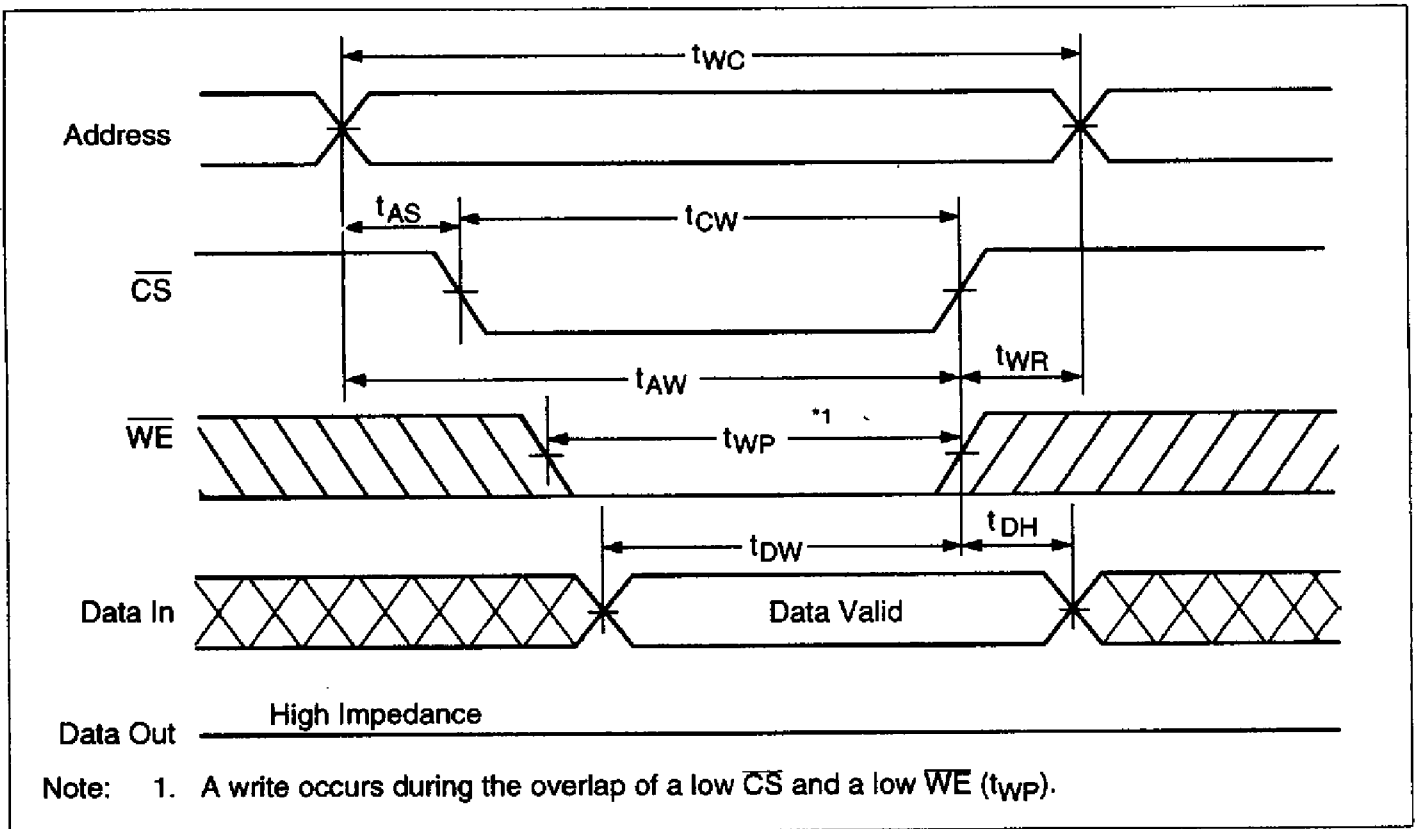
- Notes:
1. $\overline{WE} = V_{IH}$
 2. $\overline{OE} = V_{IL}$
 3. Address valid prior to or coincident with \overline{CS} transition low.

Write Cycle (1) *1 ($\overline{OE} = H, \overline{WE}$ Controlled)

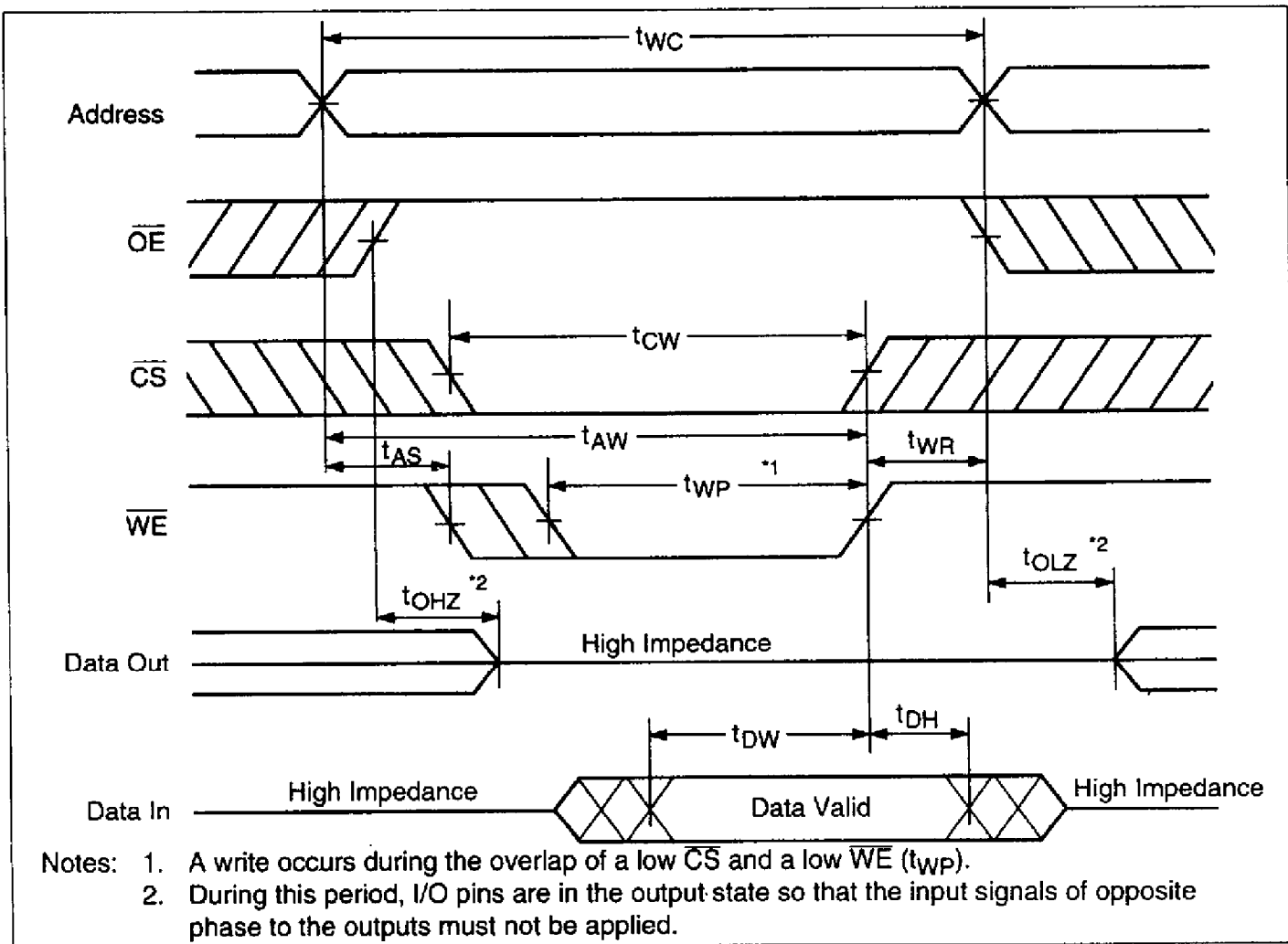


- Note: 1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} (t_{WP}).

Write Cycle (2) *1 ($\overline{OE} = H, \overline{CS}$ Controlled)

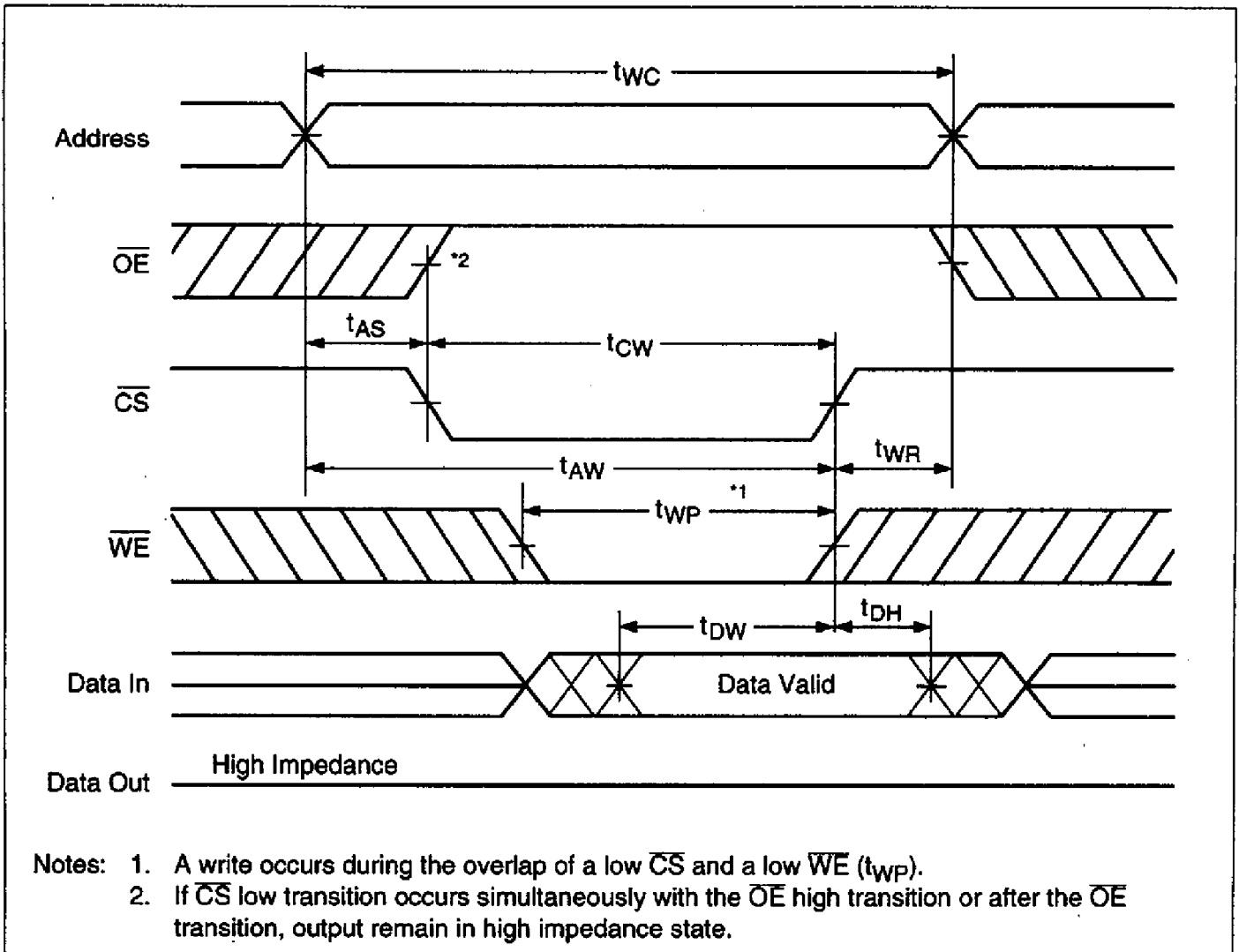


Write Cycle (3) *1, *2 ($\overline{OE} =$ Clocked, \overline{WE} Controlled)

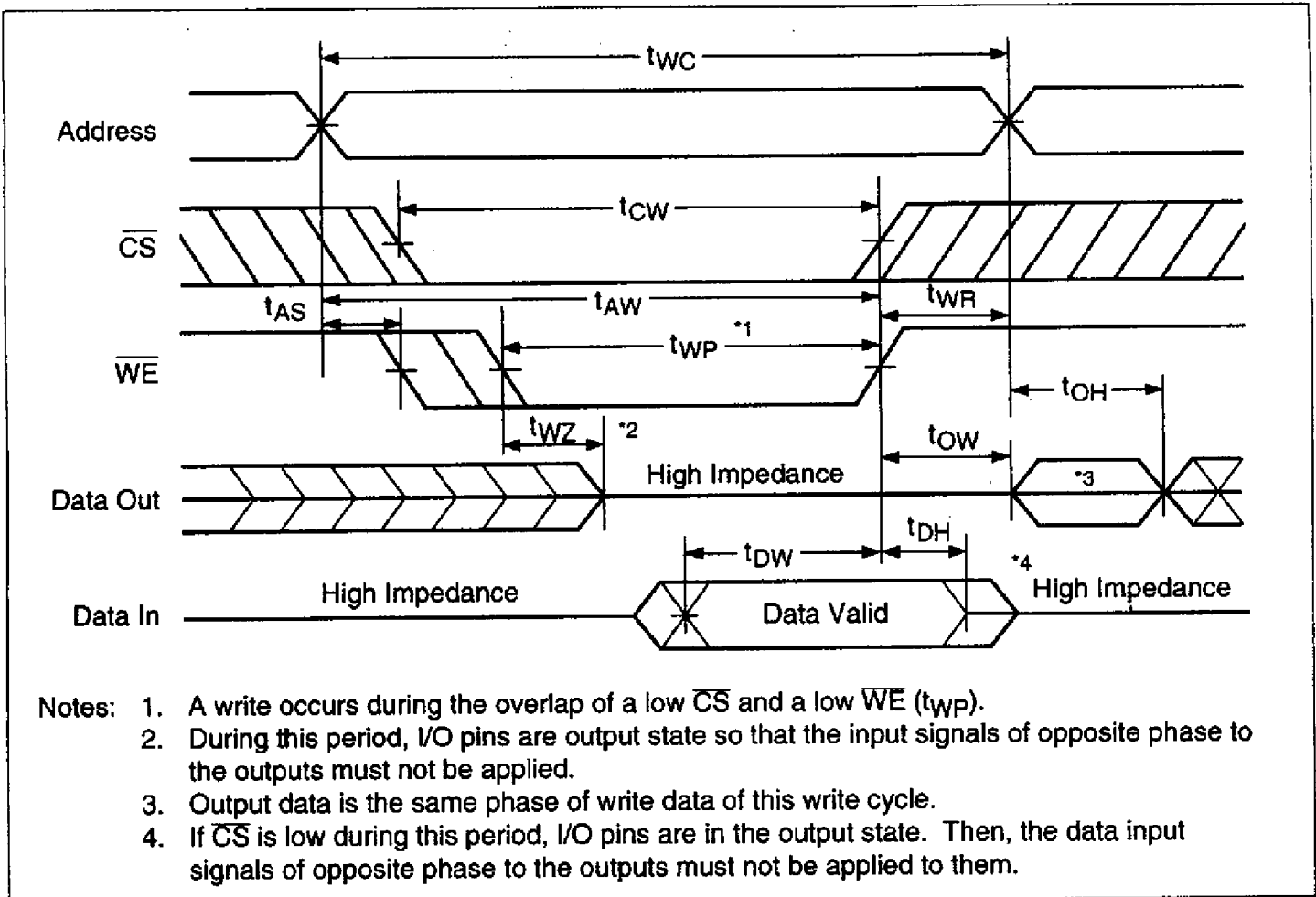


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Write Cycle (4) *1, *2 (\overline{OE} = Clocked, \overline{CS} Controlled)



- Notes:
1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} (t_{WP}).
 2. If \overline{CS} low transition occurs simultaneously with the \overline{OE} high transition or after the \overline{OE} transition, output remain in high impedance state.

Write Cycle (5) *1, *2, *3, *4 ($\overline{OE} = L$, \overline{WE} Controlled)

Write Cycle (6) *1, *2 ($\overline{OE} = L$, \overline{CS} Controlled)

